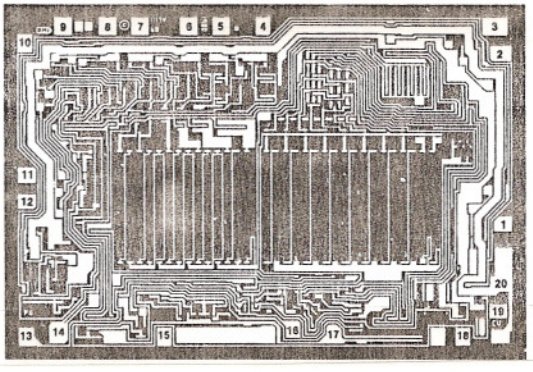
ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



1. B1 (MSB)	11. B11
2. B2	12. B12 (LSB)
3. B3	13. V_{LC}/A_{GND}
4. B4	14. V_{REF} (+)
5. B5	15. V_{REF} (−)
6. B6	16. COMP
7. B7	17. V−
8. B8	18. I_O
9. B9	19. $\overline{I_O}$
10. B10	20. V+

Topside Metal: Al
Backside: Si
Backside Potential: v+
Mask Ref: -
Bond Pads : .004" x .005"

APPROVED BY: CD	**DIE SIZE : .141" x .096"**	**DATE: 6/26/02**
MFG: Analog	**THICKNESS: .020"**	**P/N: DAC312**